

### **AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions and listings of claims in the application.

1-22. (Cancelled)

23. (Currently Amended) An integrated circuit device, comprising:

an integrated circuit die having a plurality of solder pads used for conveying signals to and from the die, the integrated circuit having a plurality of blocks of circuitry;

a substrate having a plurality of solder pads corresponding to at least a portion of the integrated circuit die's solder pads;

a plurality of solder bumps connecting the substrate to the integrated circuit die;

wherein at least one of the blocks of circuitry can be selectively configured by selectively making an electrical connection between the substrate and the integrated circuit die, the block of circuitry to be selectively configured having at least one solder pad that is used to selectively connect to the block of circuitry in order to configure the block of circuitry;

and

wherein the at least one of the blocks of circuitry is selectively configured by ~~virtue of~~ omission of a solder bump on the substrate for at least one connection between the substrate and the at least one of the ~~plurality of~~ blocks of circuitry.

24. (Original) The apparatus according to claim 23, wherein the one of the plurality of blocks of circuitry is disabled by omission of a solder bump that supplies power supply voltage to the at least one of the block of circuitry.

25. (Original) The apparatus according to claim 24, wherein the block of circuitry that is disabled is identified by testing the plurality of blocks of circuitry for functionality.

26. (Original) The apparatus according to claim 24, wherein the block of circuitry that is disabled is determined to not be functional by said testing.

27. (Original) The apparatus according to claim 24, wherein the block of circuitry that is disabled comprises one of a plurality of microprocessor cores.

28. (Original) The apparatus according to claim 24, wherein the block of circuitry that is disabled comprises at least one of a plurality of memory blocks.

29. (Original) The apparatus according to claim 24, wherein the block of circuitry that is disabled comprises one of a plurality of redundant blocks of circuitry.

30. (Original) The apparatus according to claim 24, wherein one of the plurality of solder bumps connects the substrate to a ground node in the block of circuitry that is disabled.

31. (Original) The apparatus according to claim 23, wherein the omitted solder bump, if present, would connect the substrate to a logic input forming a part of the block of circuitry.

32. (Original) The apparatus according to claim 23, wherein the substrate forms part of a chip carrier.

33. (Original) The apparatus according to claim 23, wherein the one of the plurality of blocks of circuitry is configured by selective connection of a signal to a logic gate.